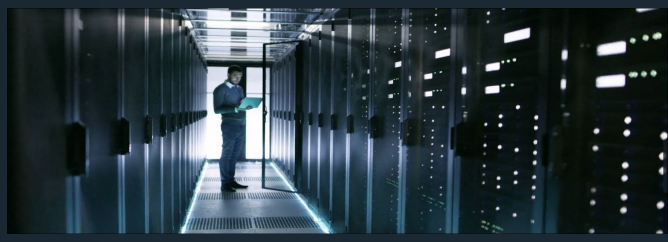
Tektronix®

Efficient Verification and Debugging for DDR5 Memory Interfaces

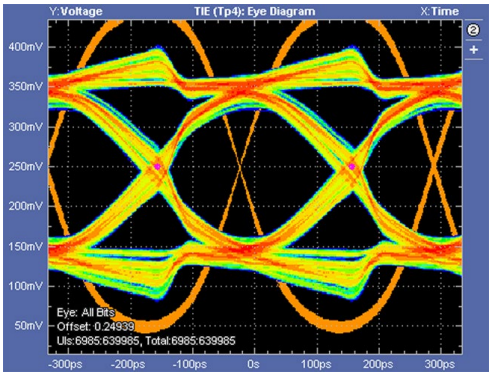


Memory tech is advancing quickly – can your measurement tools keep up?

5G is developing quickly and it's driving growth in a variety of exciting technologies – from augmented reality and artificial intelligence to cloud computing and IoT. All that data has to be stored somewhere and accessed faster than ever, meaning technology like DDR5 has never been more important. DDR5 improves bandwidth, density and channel efficiency, but higher data transfer rates and faster signal speeds mean complex designs that push the boundaries of signal integrity and require higher performance measurements for compliance, debugging and validation.

The Tektronix TekExpress DDR5 Transmitter Solution is an automated system-level test application that lets you quickly, efficiently and reliably validate and debug DDR5 designs to meet more than 50 electrical and timing measurements as defined in JEDEC.

DFE Analysis



The best tools for debugging DDR3/4 are insufficient when testing DDR5 designs in the presence of inter-symbol interference (ISI). Our DDR5 system level compliance software provides a variety of automated tools to overcome the challenges that come with the next generation of DDR including:

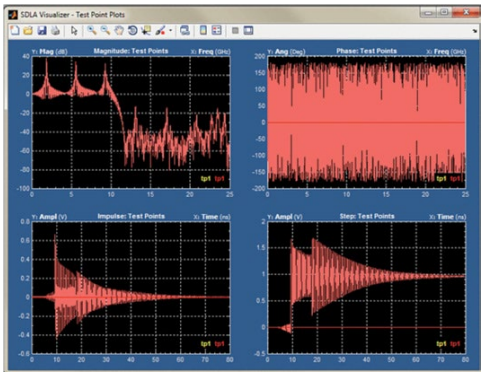
- Rx DFE Equalization support for the write data eye measurement on the bursty DDR5 traffic
- Automated measurement for 50+ DDR5 electrical and timing parameters as defined in JEDEC
- New algorithms to consistently and reliably differentiate between read and write bursts
- New compliance application architecture with enhanced automation to reduce test time and help you bring your designs to market faster.

Debugging and Validation

The TekExpress DDR5 Transmitter Solution puts control back where it should be, with the user. User defined acquisition mode allows you to run DDR5 JEDEC compliance measurements by customizing scope settings like sample rate, record length, bandwidth and more.

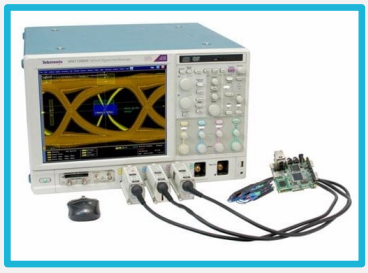
Our standalone DDR5 DFE application provides total control over the DFE Gain and 4 tap values. This allows you to run your own internal test plans – not defined or controlled by JEDEC. It also allows you to perform simulation of measurement correlation to fine tune simulation models and conduct what-if analysis by changing 4-tap and gain values.

SDLA



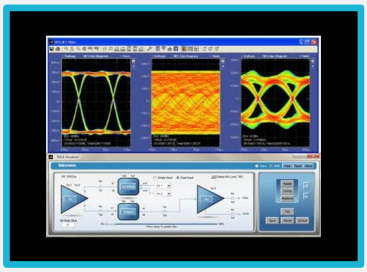
Validating s-parameters is often the primary concern when de-embedding DDR5 designs. With improved passivity checking, port assignments and plotting capabilities, not only does Serial Data Link Analysis (SDLA) enhance s-parameter file validation, it improves flexibility, saves time and increases confidence in the de-embedding process. Other debug software tools require you to complete the entire process to find results. The TekExpress DDR5 Transmitter Solution lets you detect problems at an earlier stage, allowing you to debug and optimize your designs more efficiently. SDLA features can also be helpful for DFE analysis.

For more information check out our SDLA app note here.



DDR5 Electrical Verification and Debug

View our datasheet for a deeper dive into the TekExpress DDR5 Transmitter Solution software and how it can help you analyze and optimize complex DDR5 designs with ease.



Serial Data Link Analysis Visualizer

SDLA Visualizer measurement circuit software runs directly on an oscilloscope and provides extensive capability for computing embed and de-embed filters for real-time measurement and simulation.

P7700 Series TriMode Probes

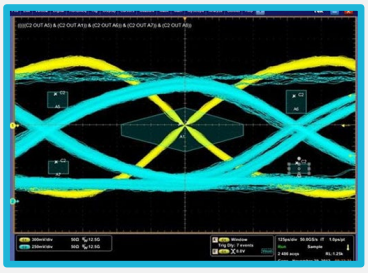
P7700 Series Trimode Probes provide unmatched usability for challenging electronic designs. **New P77STFLRB** and **P77HTFLRB** solder-in tips improve signal access and reduce mechanical strain relief.

DPO70000SX ATI Oscilloscope

DPO70000SX ATI Performance Oscilloscopes deliver the industry's most accurate capture of high-speed signal behavior to verify, validate and characterize your next generation designs.

MSO/DPO70000 Oscilloscope

Discover your real signals and capture more of their details with the industry's highest waveform capture capability. Automate setup, acquisition and analysis of high-speed serial data signals.



TekExpress Compliance/Debug

The Tektronix TekExpress DDR Tx is an automated test application used to validate and debug the DDR5 and LPDDR5 designs of the DUT as per the JEDEC specifications.

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