

# quantumdata™ M41h

## 48G Video Analyzer/Generator for HDMI Testing

Deep Analysis & Generation of HDMI 2.1 Fixed Rate Link (FRL) w/ Forward Error Correction (FEC)  
Entry Level Functional Tester Upgradable to Full Compliance



### Key Features

- Verify the 16b/18b encoding for Fixed Rate Link (FRL) Packets in both 3 and 4 lane configurations
- Use generator or analyzer in three (3) Lane configuration mode at 3Gbps & 6Gbps data rates and four (4) Lane configurations at 6Gbps, 8Gbps, 10Gbps and 12Gbps (48Gbps aggregate)
- Video generator function supports TMDS and FRL for video resolutions up to 8K at 1485MHz pixel rates
- View captured data elements graphically in Event Plot and in Data Decode Table; use searching and filtering to find data
- View FRL packet mapping into Character Blocks and Character Block (including FEC characters) mapping into Super Blocks
- Run complete suite of FRL source & sink compliance tests
- Run eARC the full suite of compliance tests on an eARC Tx or Rx device; all tests supported
- Run complete suite of TMDS source & sink compliance tests
- Run complete suite of HDCP 2.3 source, sink & repeater compliance tests
- View TMDS video and protocol elements, data island blocks, preamble data and sync control elements
- Monitor of FRL Link Training transactions in the Auxiliary Channel Analyzer (ACA) utility to show SCDC reads and writes over the DDC channel
- View Lane Error Counts and Reed Solomon Corrections Count in the SCDC CED registers
- Verify the eARC common mode channel on either an eARC Tx or Rx device
- Provides an extensive command line API to support automated testing

The Teledyne LeCroy quantumdata M41h 48Gbps Video Analyzer / Generator for HDMI Testing is a compact, versatile test instrument that can be easily extended from an entry level functional tester to a full certified compliance tester. The M41h is equipped with both HDMI Tx and Rx ports supporting HDMI 2.1 Fixed Rate Link and FEC capture analysis and decode up to 48Gbps (12Gbps/Lane). The HDMI Rx analyzer port provides visibility into the Fixed Rate Link packetization –super blocks, character blocks and FRL packets and underlying TMDS video, protocol, control and metadata elements. The HDMI Tx video generator port transmits Fixed Rate Link video streams with embedded TMDS video, protocol, control and metadata elements. The M41h also supports the full suite of FRL source and sink compliance tests as well as Enhanced Audio Return Channel (eARC) compliance testing for both Tx and Rx devices. An extensive Application Programming Interface (API) is supported for automated testing systems available thru a command line interface.

### Operation

The M41h supports video generation and analysis of the FRL/FEC HDMI data streams through the user friendly GUI Manager which presents the data in an easy to understand way. The GUI can be controlled either via a laptop connected to the M41h RJ45 LAN port or through a USB keyboard and mouse and a connected UHD HDMI admin display.

### Admin display for ATP Mgr



### M41h 48Gbps Video Analyzer / Generator

Keyboard & mouse for ATP Manager control

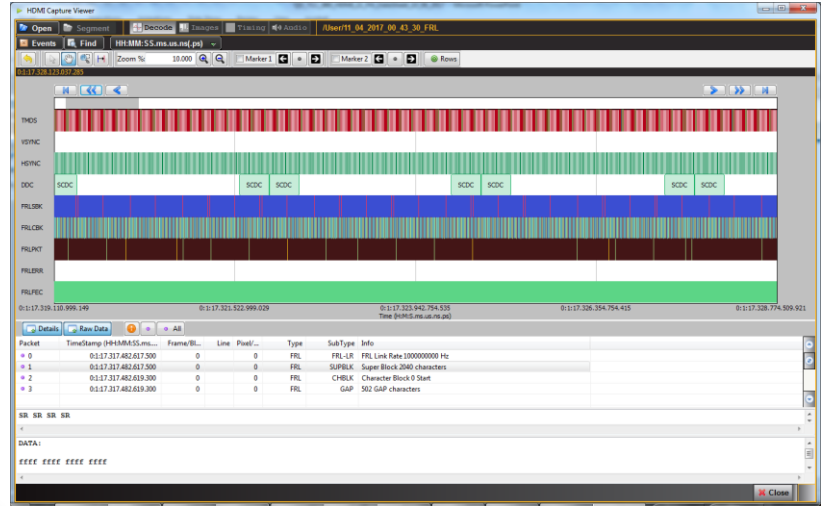


# FIXED RATE LINK (FRL) CAPTURE/DECODE ANALYSIS

## Capture and Decode (FRL & FEC)

The M41h analyzer captures and decodes incoming HDMI 2.1 streams that have been packetized with FRL packet structures. These FRL-related data elements are depicted graphically in the Event Plot. The decoded data and the raw data is shown in table form in the Data Decode window. The Forward Error Correction (FEC) characters are also shown as well. The module reports the Lane Error Counts and the FEC Reed Solomon Corrections Count in the SCDC CED registers. The underlying TMDS video and protocol elements such as the active video, data island and preamble blocks, are also depicted and decoded. Each element is assigned a precise time stamp. Users can search and filter the FRL captured data by type.

## Capture Showing SCDC, FRL & TMDS Elements



Admin Display for M41h GUI

HDMI 2.1 FRL-Capable Source DUT

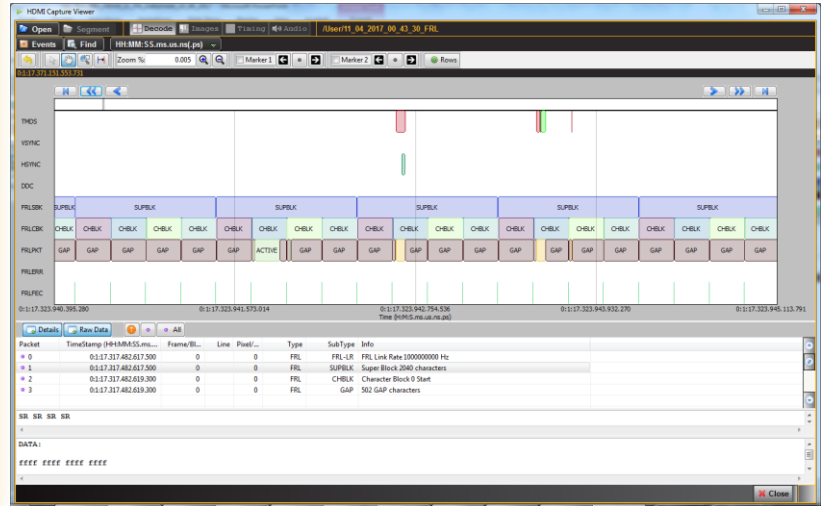


M41h

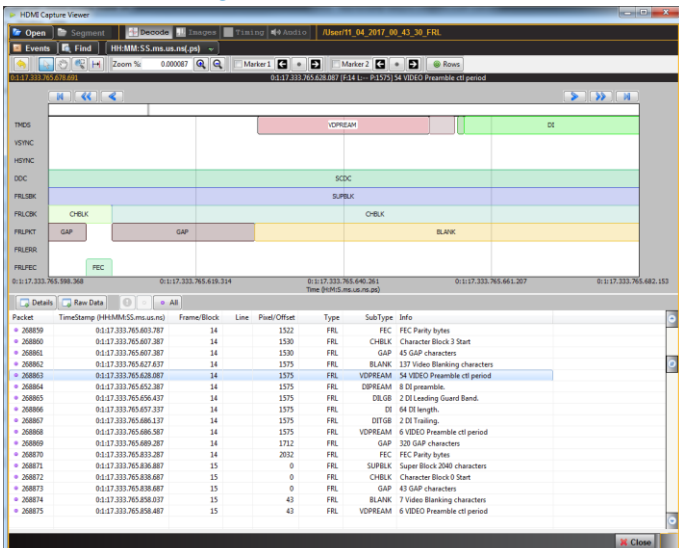


Test Setup for Source Test

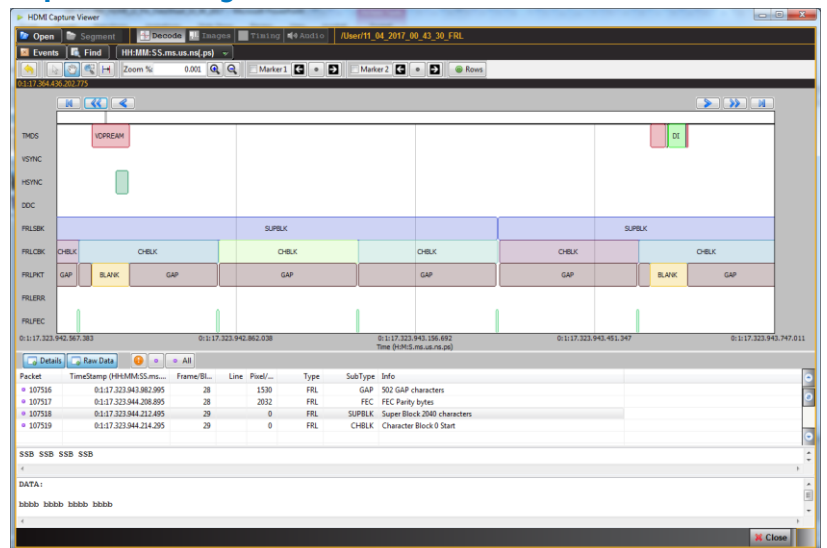
## Capture Showing FRL Packets, Character & Super Blocks



## Capture Showing Active Video Elements and FEC



## Capture Showing FRL Elements & TMDS Video & Data

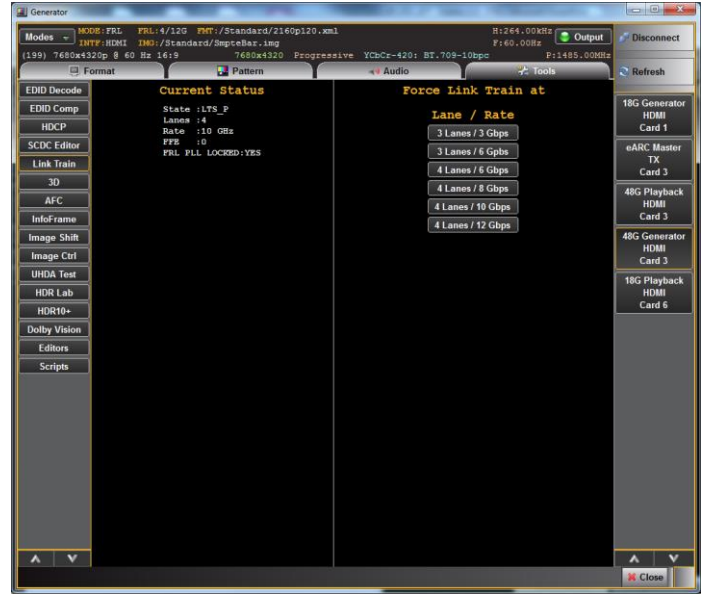


# FIXED RATE LINK (FRL) LINK TRAINING ANALYSIS

## Link Training

The M41h supports Link Training configuration and control. The module emulates an HDMI 2.1 sink indicating the max FRL rate in the HF-VSDB of the EDID and various other essential link training parameters in the SCDC control registers.

## Generator Link Training Status & Control Screen



Admin Display for ATP Manager

HDMI 2.1 FRL-Capable Source device under test

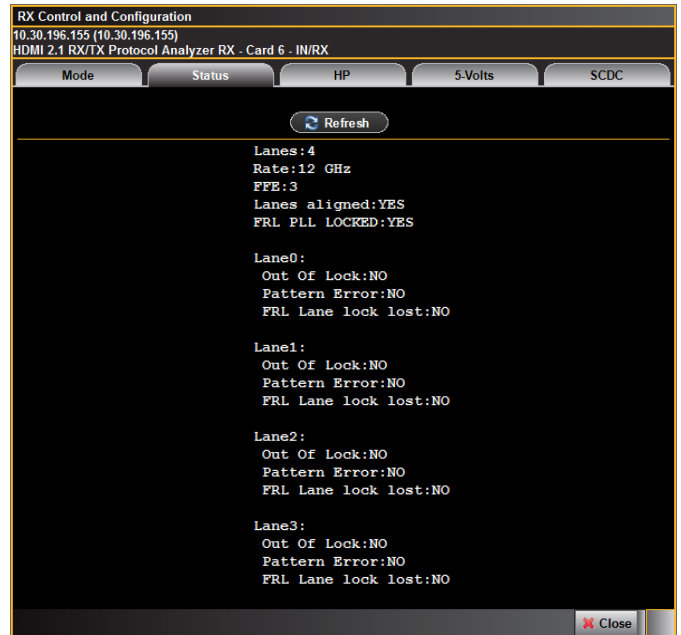


Test Setup for Source Test

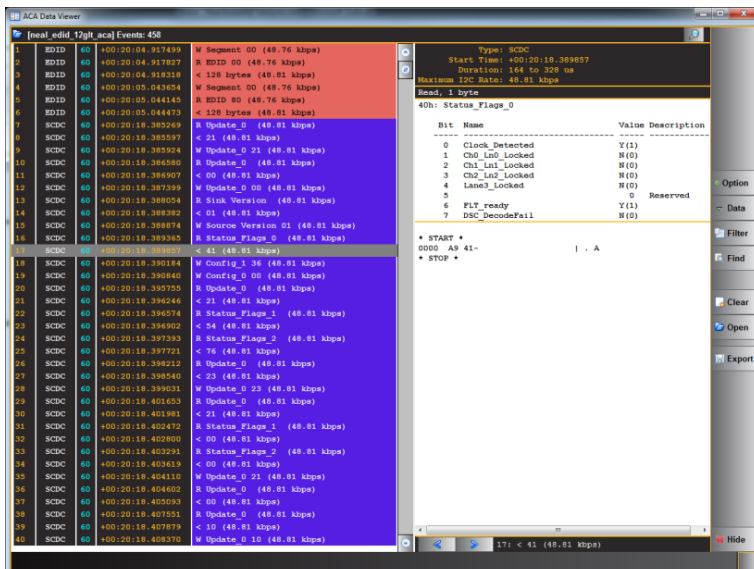
## Auxiliary Channel Analyzer

You can use the M41h to monitor the Link Training transactions—EDID exchange and reads and writes to the SCDC registers over the DDC channel—with the Aux Channel Analyzer (ACA) utility. This enables you to verify link training functions to identify potential interoperability problems.

## Analyzer Link Training Status Screen



## Auxiliary Channel Analyzer (Link Training over DDC)



# FIXED RATE LINK (FRL) VIDEO GENERATION

## FRL Video Generation

The M41h for HDMI Testing enables developers of HDMI and TMDS FRL-capable sink devices and silicon makers to run functional tests on their FRL-capable display devices by rendering uncompressed, unencrypted FRL streams at up to 8K video resolutions at lane rates up to 12Gb/s and at an aggregate link rate of 48Gb/s and up to pixel rates of 1485MHz. The enhanced video generator function enables specific selections of video formats, colorimetry, bit depth, chroma subsampling, color space and test patterns.

HDMI 2.1  
FRL-Capable  
UHD TV DUT



M41h

Host PC  
for ATP  
Manager



Display (Sink)  
Test Setup

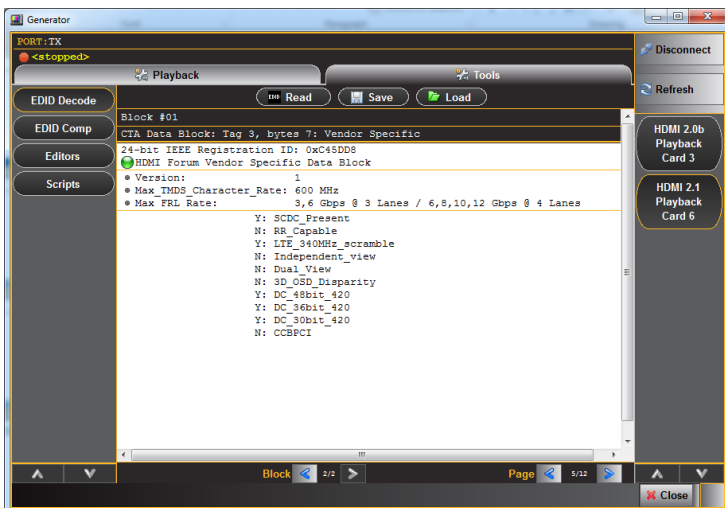
## Link Training Configuration

The M41h's video generation function enables you to configure the lane rate and number of lanes for transmission of the FRL stream.

## EDID Read

The M41h enables you to view the EDID of the connected display (below). You can page through each block and save for later viewing.

## Reading the EDID



## Selection of FRL and TMDS Video Resolutions



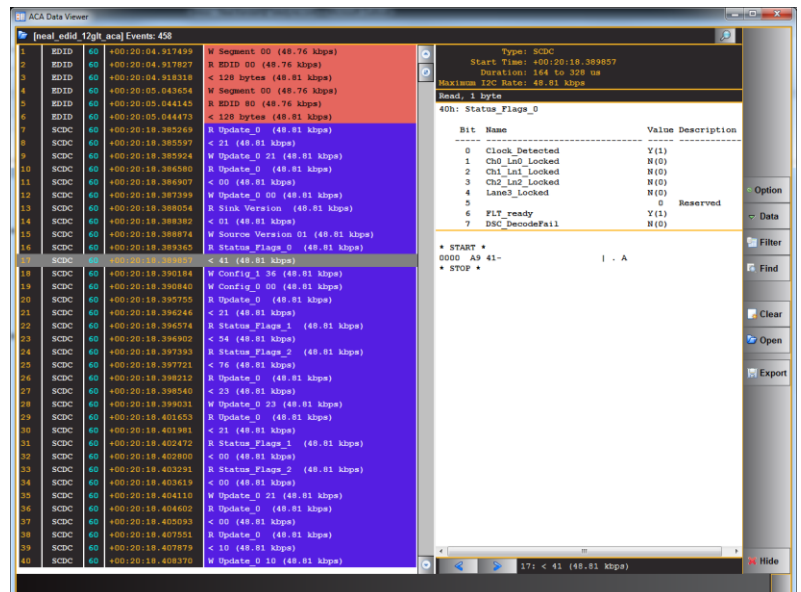
## Link Training Configuration



## Auxiliary Channel Analyzer (ACA)

You can use the M41h to monitor the Link Training transactions—EDID exchange and reads and writes to the SCDC registers over the DDC channel—with the Aux Channel Analyzer utility. The FRL link training transactions enable developers to verify that their displays are properly conducting their role in the link training process.

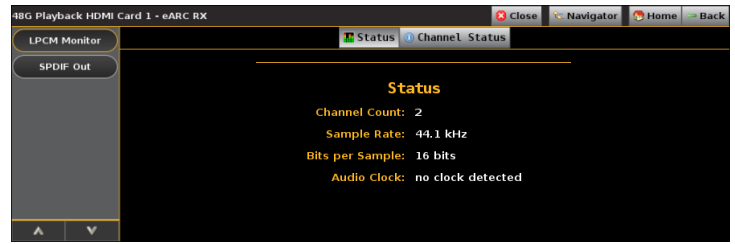
## Auxiliary Channel Analyzer (Link Training)



# eARC FUNCTIONAL AND COMPLIANCE TESTING

## eARC Functional Testing

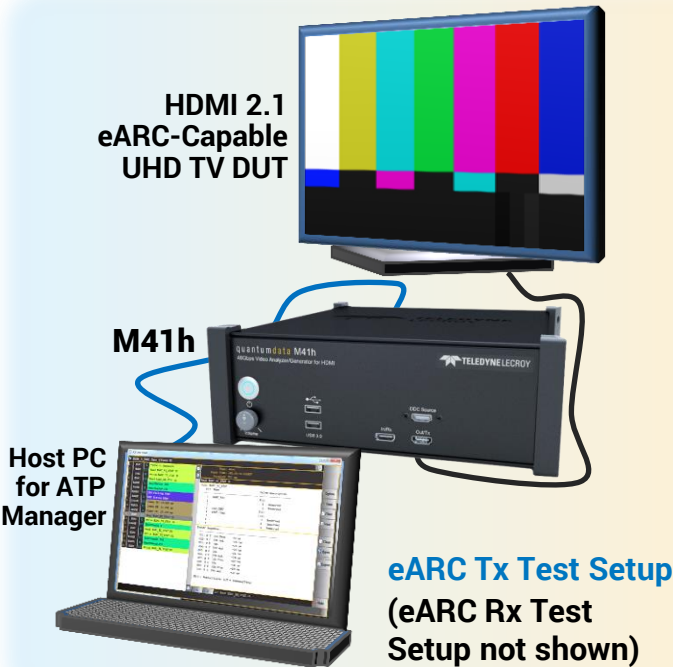
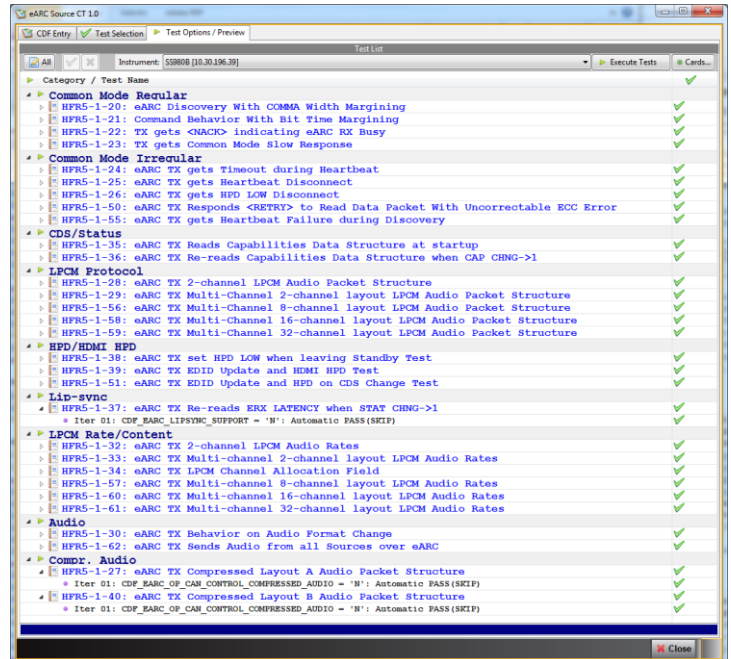
The 48G Video Analyzer / Generator is also supports enhanced Audio Return Channel (eARC) Tx/Rx functional testing. The solution provides emulation of an eARC Tx and Rx functions over the eARC Common Mode and Differential mode data channels. Solution supports discovery and disconnect, heartbeat, status and capabilities data structure and transmission over the differential channel. (Sample screen showing monitoring incoming audio stream, right.)



## eARC Compliance Testing

The M41h enables developers of HDMI eARC Tx and Rx devices to run compliance tests on their eARC-capable. The compliance tests run with little or no human interaction. Detailed results are provided for each test to help identify the root cause of failures. The reports can be exported and disseminated to colleagues and other subject matter experts.

## Test Suite (eARC Tx Test Suite Example Shown)

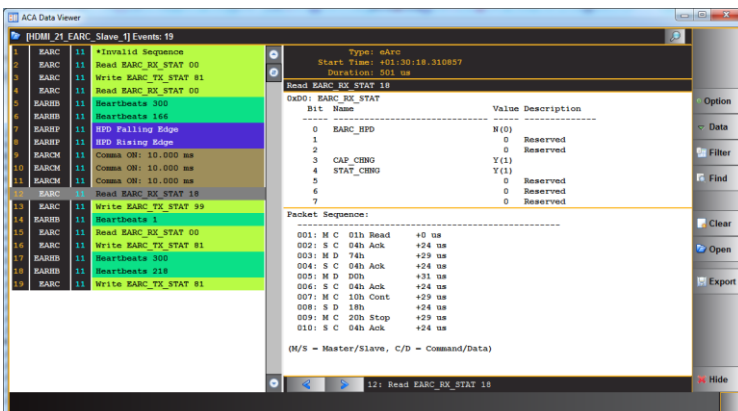


eARC Tx Test Setup  
(eARC Rx Test Setup not shown)

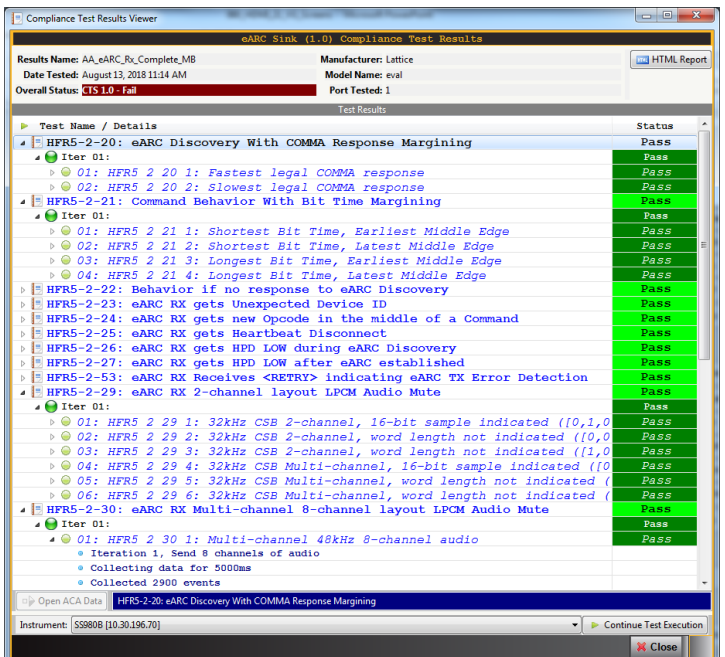
## Auxiliary Channel Analyzer (ACA)

The M41h can monitor the Link Training transactions—EDID exchange and reads and writes to the SCDC registers over the DDC channel -with the Aux Channel Analyzer (ACA) utility. Viewing the FRL link training transactions enables developers to verify their displays are properly conducting the link training process properly.

## Aux Chan Analyzer Traces (Common Mode Discovery)



## Sample eARC Test Results (eARC Rx Tests Shown)



# FIXED RATE LINK (FRL) SOURCE COMPLIANCE

## FRL Source Compliance Testing

The M41h for HDMI Testing enables developers of HDMI FRL-capable source devices and silicon makers to run compliance tests on their FRL-capable source devices on unencrypted FRL streams at up to 8K video resolutions at lane rates up to 12Gb/s and at an aggregate link rate of 48Gb/s. All compliance test data, including the captured data, is exportable and can be disseminated to colleagues and other subject matter experts.

Admin Display for ATP Manager

HDMI 2.1 FRL-Capable Source device under

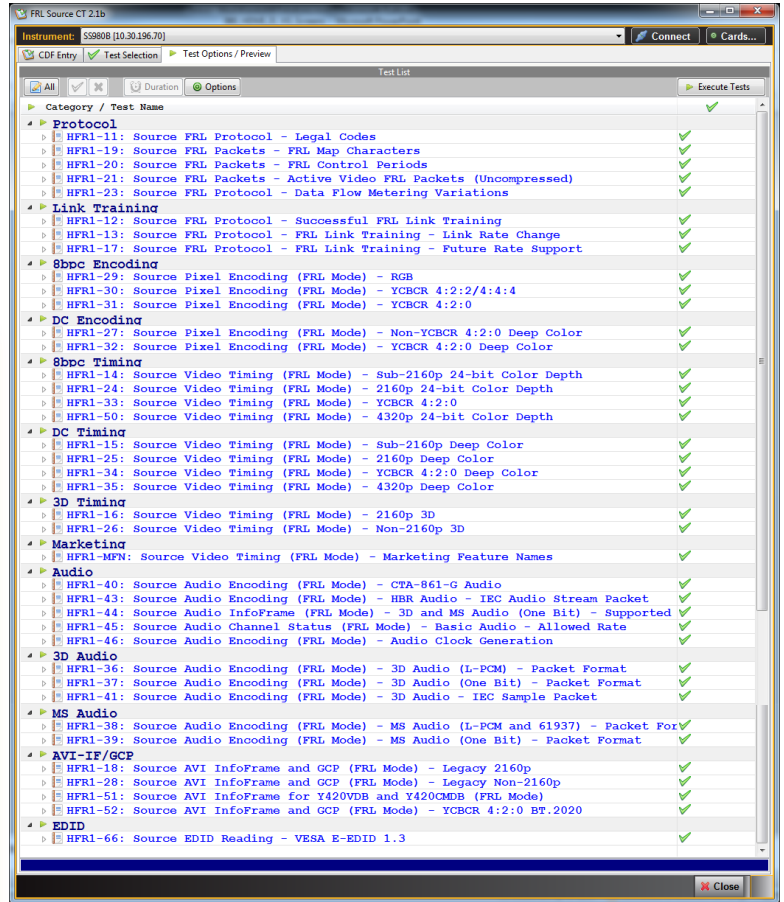


M41h

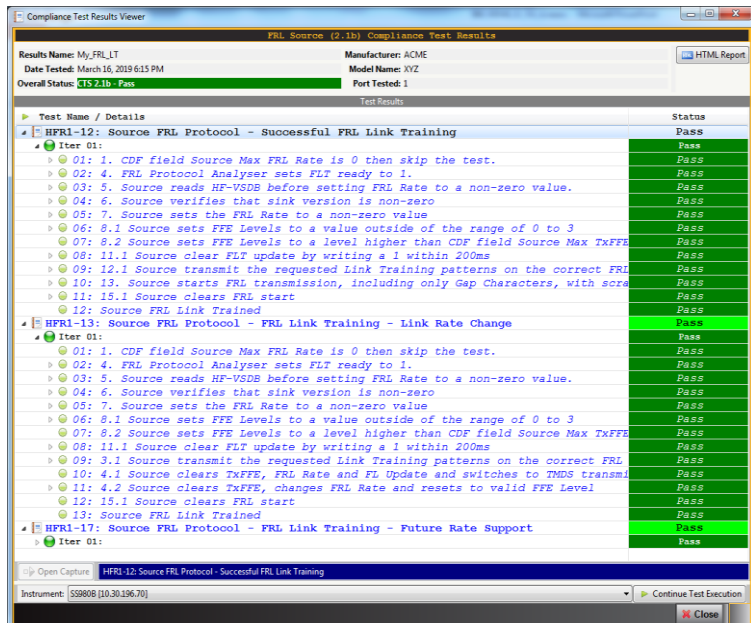


Test Setup for Source Test

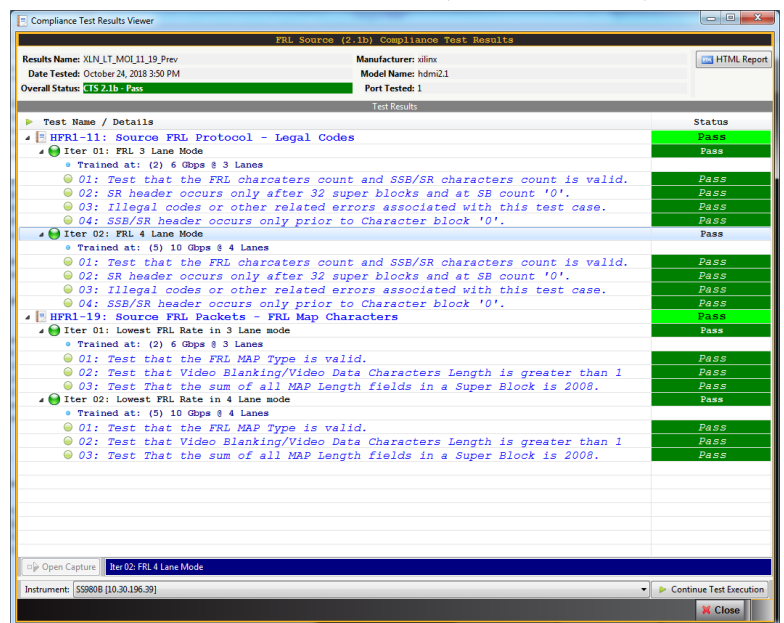
## Selection of FRL Source Compliance tests



## Sample FRL Source Compliance (Link Training Tests)



## Sample FRL Source Compliance (Protocol Tests)

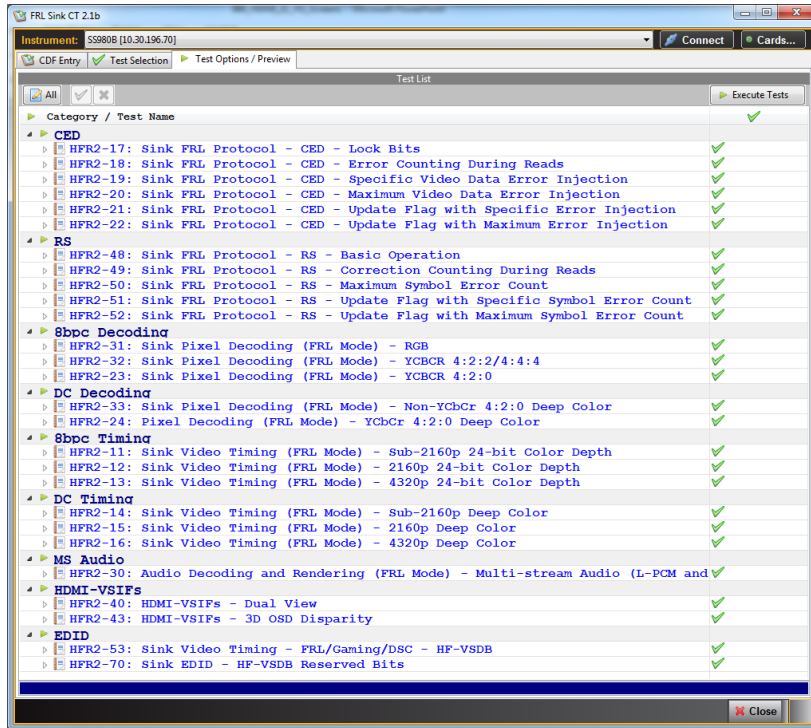


# FIXED RATE LINK (FRL) SINK COMPLIANCE

## FRL Sink Compliance Testing

The M41h for HDMI Testing enables developers of HDMI FRL-capable sink devices and silicon makers to run compliance tests on their FRL-capable sink devices with FRL streams at up to 8K video resolutions at lane rates up to 12Gb/s and at an aggregate link rate of 48Gb/s and pixel rates up to 1485MHz. All compliance test data, including the captured data, is exportable and can be disseminated to colleagues and other subject matter experts.

## Selection of FRL Sink Compliance tests



Category / Test Name	Status
<b>CED</b>	
HFR2-17: Sink FRL Protocol - CED - Lock Bits	Pass
HFR2-18: Sink FRL Protocol - CED - Error Counting During Reads	Pass
HFR2-19: Sink FRL Protocol - CED - Specific Video Data Error Injection	Pass
HFR2-20: Sink FRL Protocol - CED - Maximum Video Data Error Injection	Pass
HFR2-21: Sink FRL Protocol - CED - Update Flag with Specific Error Injection	Pass
HFR2-22: Sink FRL Protocol - CED - Update Flag with Maximum Error Injection	Pass
<b>RS</b>	
HFR2-48: Sink FRL Protocol - RS - Basic Operation	Pass
HFR2-49: Sink FRL Protocol - RS - Correction Counting During Reads	Pass
HFR2-50: Sink FRL Protocol - RS - Maximum Symbol Error Count	Pass
HFR2-51: Sink FRL Protocol - RS - Update Flag with Specific Symbol Error Count	Pass
HFR2-52: Sink FRL Protocol - RS - Update Flag with Maximum Symbol Error Count	Pass
<b>8bpc Decoding</b>	
HFR2-31: Sink Pixel Decoding (FRL Mode) - RGB	Pass
HFR2-32: Sink Pixel Decoding (FRL Mode) - YCbCr 4:2:2/4:4:4	Pass
HFR2-23: Sink Pixel Decoding (FRL Mode) - YCbCr 4:2:0	Pass
<b>DC Decoding</b>	
HFR2-33: Sink Pixel Decoding (FRL Mode) - Non-YCbCr 4:2:0 Deep Color	Pass
HFR2-24: Pixel Decoding (FRL Mode) - YCbCr 4:2:0 Deep Color	Pass
<b>8bpc Timing</b>	
HFR2-11: Sink Video Timing (FRL Mode) - Sub-2160p 24-bit Color Depth	Pass
HFR2-12: Sink Video Timing (FRL Mode) - 2160p 24-bit Color Depth	Pass
HFR2-13: Sink Video Timing (FRL Mode) - 4320p 24-bit Color Depth	Pass
<b>DC Timing</b>	
HFR2-14: Sink Video Timing (FRL Mode) - Sub-2160p Deep Color	Pass
HFR2-15: Sink Video Timing (FRL Mode) - 2160p Deep Color	Pass
HFR2-16: Sink Video Timing (FRL Mode) - 4320p Deep Color	Pass
<b>MS Audio</b>	
HFR2-30: Audio Decoding and Rendering (FRL Mode) - Multi-stream Audio (L-PCM and	Pass
<b>HDMI-VSIFs</b>	
HFR2-40: HDMI-VSIFs - Dual View	Pass
HFR2-43: HDMI-VSIFs - 3D OSD Disparity	Pass
<b>EDID</b>	
HFR2-53: Sink Video Timing - FRL/Gaming/DSC - HF-VSDB	Pass
HFR2-70: Sink EDID - HF-VSDB Reserved Bits	Pass

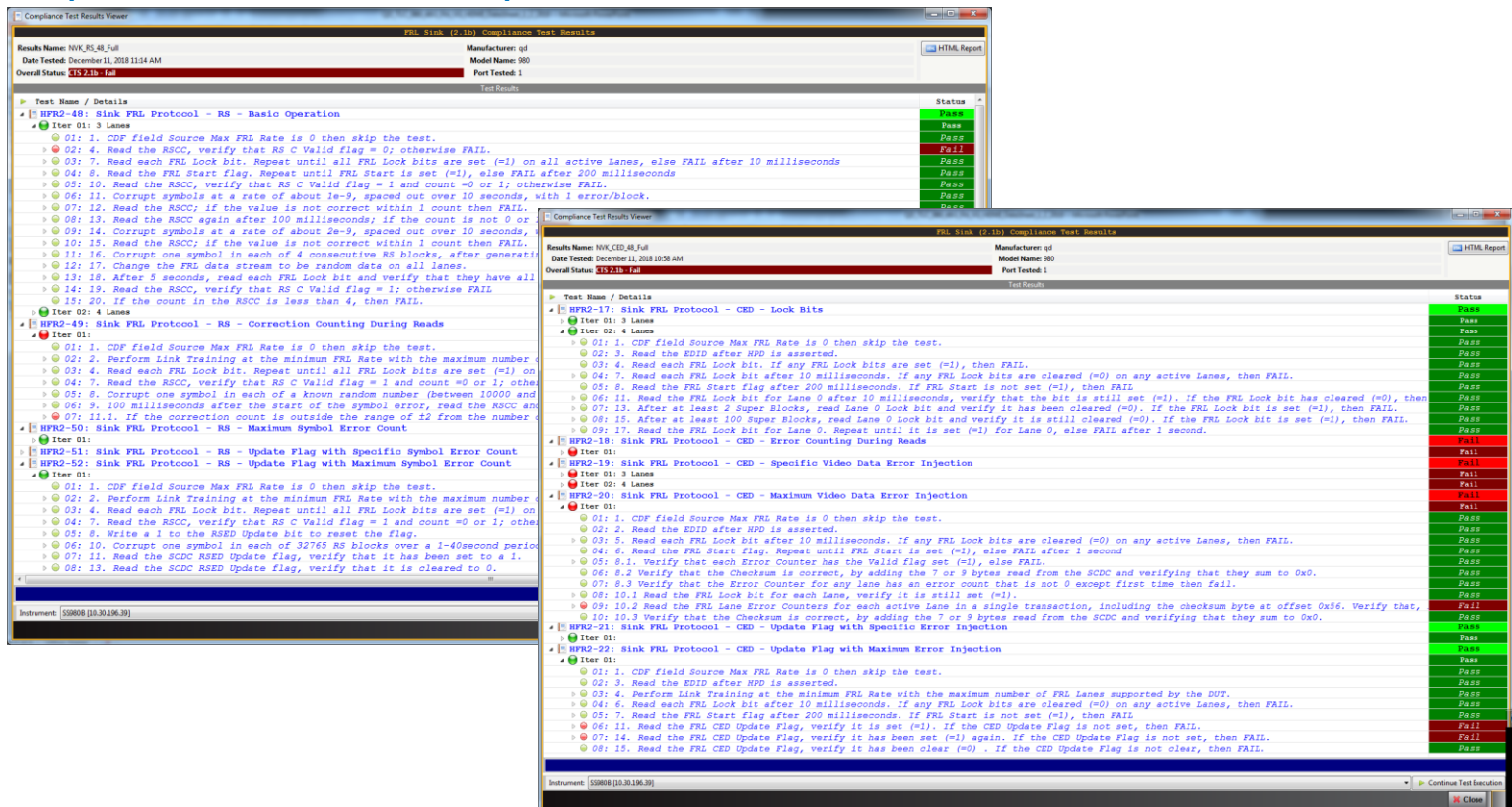
HDMI 2.1  
FRL-Capable  
UHD TV DUT

M41h

Host PC  
for ATP  
Manager

Sink CT Test Setup

## Sample Test Results of FRL Sink Compliance tests



Test Name / Details	Status
<b>HFR2-48: Sink FRL Protocol - RS - Basic Operation</b>	Pass
01: 1. CDF field Source Max FRL Rate is 0 then skip the test.	Pass
02: 4. Read the RS CC Valid flag = 0; otherwise FAIL.	Pass
03: 7. Read each FRL Lock bit. Repeat until all FRL Lock bits are set (=1) on all active Lanes, else FAIL after 10 milliseconds	Pass
04: 8. Read the FRL Start flag. Repeat until FRL Start is set (=1), else FAIL after 200 milliseconds	Pass
05: 10. Read the RS CC, verify that RS C Valid flag = 1 and count = 0 or 1; otherwise FAIL.	Pass
06: 11. Corrupt symbols at a rate of about 1e-9, spaced out over 10 seconds, with 1 error/block.	Pass
07: 12. Read the RS CC; if the value is not correct within 1 count then FAIL.	Pass
08: 13. Read the RS CC again after 100 milliseconds; if the count is not 0 or 1.	Pass
09: 14. Corrupt symbols at a rate of about 2e-9, spaced out over 10 seconds.	Pass
10: 15. Read the RS CC; if the value is not correct within 1 count then FAIL.	Pass
11: 16. Corrupt one symbol in each of 4 consecutive RS blocks, after generating 12: 17. Change the FRL data stream to be random data on all lanes.	Pass
13: 18. After 5 seconds, read each FRL Lock bit and verify that they have all	Pass
14: 19. Read the RS CC, verify that RS C Valid flag = 1; otherwise FAIL	Pass
15: 20. If the count in the RS CC is less than 4, then FAIL.	Pass
<b>HFR2-49: Sink FRL Protocol - RS - Correction Counting During Reads</b>	Pass
01: 1. CDF field Source Max FRL Rate is 0 then skip the test.	Pass
02: 2. Perform Link Training at the minimum FRL Rate with the maximum number	Pass
03: 4. Read each FRL Lock bit. Repeat until all FRL Lock bits are set (=1) on	Pass
04: 7. Read the RS CC, verify that RS C Valid flag = 1 and count = 0 or 1; other	Pass
05: 8. Corrupt one symbol in each of a known random number (between 10000 and	Pass
06: 9. 100 milliseconds after the start of the symbol error, read the RS CC and	Pass
07: 11. If the correction count is outside the range of 12 from the number	Pass
<b>HFR2-50: Sink FRL Protocol - RS - Maximum Symbol Error Count</b>	Pass
<b>HFR2-51: Sink FRL Protocol - RS - Update Flag with Specific Symbol Error Count</b>	Pass
<b>HFR2-52: Sink FRL Protocol - RS - Update Flag with Maximum Symbol Error Count</b>	Pass
01: 1. CDF field Source Max FRL Rate is 0 then skip the test.	Pass
02: 2. Perform Link Training at the minimum FRL Rate with the maximum number	Pass
03: 4. Read each FRL Lock bit. Repeat until all FRL Lock bits are set (=1) on	Pass
04: 7. Read the RS CC, verify that RS C Valid flag = 1 and count = 0 or 1; other	Pass
05: 8. Corrupt one symbol in each of 32768 RS blocks over a 1-40second period	Pass
07: 11. Read the RS CC RSED Update flag, verify that it has been set to a 1.	Pass
08: 13. Read the RS CC RSED Update flag, verify that it is cleared to 0.	Pass
<b>HFR2-17: Sink FRL Protocol - CED - Lock Bits</b>	Pass
01: 1. CDF field Source Max FRL Rate is 0 then skip the test.	Pass
02: 2. Read the EDID after HPD is asserted.	Pass
03: 3. Read each FRL Lock bit after 10 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.	Pass
04: 4. Read the FRL Start flag. Repeat until FRL Start is set (=1), else FAIL after 1 second	Pass
05: 5. Verify that each Error Counter has the Valid flag set (=1), else FAIL.	Pass
06: 6. Read the FRL Start flag after 200 milliseconds. If FRL Start is not set (=1), then FAIL	Pass
07: 7. Read the FRL Lock bit for Lane 0 after 10 milliseconds, verify that the bit is still set (=1). If the FRL Lock bit has cleared (=0), then FAIL.	Pass
08: 8. Read each FRL Lock bit after 10 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.	Pass
09: 9. After at least 10 Super Blocks, read Lane 0 Lock bit and verify it is still cleared (=0). If the FRL Lock bit is set (=1), then FAIL.	Pass
10: 10. Read the FRL Lock bit for Lane 0. Repeat until it is set (=1) for Lane 0, else FAIL after 1 second.	Pass
<b>HFR2-18: Sink FRL Protocol - CED - Error Counting During Reads</b>	Pass
<b>HFR2-19: Sink FRL Protocol - CED - Specific Video Data Error Injection</b>	Pass
<b>HFR2-20: Sink FRL Protocol - CED - Maximum Video Data Error Injection</b>	Pass
01: 1. CDF field Source Max FRL Rate is 0 then skip the test.	Pass
02: 2. Read the EDID after HPD is asserted.	Pass
03: 3. Read each FRL Lock bit after 10 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.	Pass
04: 4. Read the FRL Start flag. Repeat until FRL Start is set (=1), else FAIL after 1 second	Pass
05: 5. Verify that each Error Counter has the Valid flag set (=1), else FAIL.	Pass
06: 6. Verify that the Checksum is correct, by adding the 7 or 9 bytes read from the SCCC and verifying that they sum to 0x0.	Pass
07: 7. Read the FRL Lock bit for each Lane. Verify that each Error Counter has an error count that is not 0 except first time then fail.	Pass
08: 8. Read the FRL Lock bit for each Lane, verify it is still set (=1).	Pass
09: 10.2 Read the FRL Lane Error Counters for each active Lane in a single transaction, including the checksum byte at offset 0x56. Verify that,	Pass
10: 10.3 Verify that the Checksum is correct, by adding the 7 or 9 bytes read from the SCCC and verifying that they sum to 0x0.	Pass
<b>HFR2-31: Sink FRL Protocol - CED - Update Flag with Specific Error Injection</b>	Pass
<b>HFR2-32: Sink FRL Protocol - CED - Update Flag with Maximum Error Injection</b>	Pass
01: 1. CDF field Source Max FRL Rate is 0 then skip the test.	Pass
02: 2. Read the EDID after HPD is asserted.	Pass
03: 3. Read each FRL Lock bit after 10 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.	Pass
04: 4. Perform Link Training at the minimum FRL Rate with the maximum number of FRL Lanes supported by the DUT.	Pass
05: 5. Read each FRL Lock bit after 10 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.	Pass
06: 6. Read the FRL Start flag after 200 milliseconds. If FRL Start is not set (=1), then FAIL	Pass
07: 7. Read the FRL CED Update Flag, verify that it is set (=1). If the CED Update Flag is not set, then FAIL.	Pass
08: 8. Read the FRL CED Update Flag, verify that it has been set (=1) again. If the CED Update Flag is not set, then FAIL.	Pass
09: 9. Read the FRL CED Update Flag, verify that it has been cleared (=0). If the CED Update Flag is not cleared, then FAIL.	Pass

# HDMI 2.0 SOURCE COMPLIANCE TESTS

## HDMI 2.0 Source Compliance

The M41h source compliance tests are ideal for pre-testing your HDMI 2.0 source product prior to submission to an Authorized Test Center for approval. Pre-testing provides added assurance that your product will pass at the ATC when submitted. Where permitted, the M41h can be used to self-test your product. Self-testing offers greater benefits for time to market and cost reduction than pre-testing by avoiding submission to the ATC for approval. The compliance tests enable you to view the captured data and detailed test results which help pinpoint the cause of compliance test failures.



## HDMI 2.0 Compliance Test List

Category / Test Name	Status
<b>TMDs Protocol</b>	
HFI-10: TMDs Protocol - 6G - TMDs Bit Clock Ratio	✓
HFI-11: Source TMDs Protocol - 6G Legal Codes	✓
HFI-12: TMDs Protocol - 6G - Basic Protocol and Scrambling	✓
HFI-13: TMDs Protocol - Scrambling <= 3.4Gbps	✓
HFI-21: TMDs Protocol - 6G - Legal Codes - other Video Timings	✓
HFI-22: TMDs Protocol - 6G - Basic Protocol and Scrambling - Other Video Timings	✓
<b>Pixel Encoding</b>	
HFI-31: Pixel Encoding - YCBCR 4:2:0 - TMDs Pixel Encoding	✓
HFI-32: Pixel Encoding - YCBCR 4:2:0 Deep Color - TMDs Pixel Encoding	✓
<b>Video Timing</b>	
HFI-14: Video Timing - 6G - 2160p 24-bit Color Depth	✗
HFI-15: Video Timing - 6G - Deep Color	✓
HFI-16: Video Timing - 6G - 2160p 3D	✓
HFI-24: Video Timing - 6G - Other 24-bit Color Depth	✓
HFI-25: Video Timing - 6G - Other Deep Color	✓
HFI-26: Video Timing - 6G - Non-2160p 3D	✓
HFI-33: Video Timing - YCBCR 4:2:0	✓
HFI-34: Video Timing - YCBCR 4:2:0 Deep Color	✓
HFI-35: Video Timing - 21.9 (64:27)	✓
<b>AVI-IF/GCP</b>	
HFI-18: AVI InfoFrame - 6G	✓
HFI-28: AVI InfoFrame - 6G - Other Video Timings	✓
HFI-51: AVI InfoFrame for Y420VDB and Y420CMB	✓
HFI-52: AVI InfoFrame and GCP - YCBCR 4:2:0 BP.2020	✓
<b>HDMI-VSIFs</b>	
HFI-47: HDMI VSIFs - 3D OSD Disparity	✓
HFI-48: HDMI VSIFs - Dual-View	✓
HFI-49: HDMI VSIFs - Independent-View	✓
<b>Audio</b>	
HFI-41: Audio Encoding - 3D Audio - IEC Sample Packet	✓
HFI-43: Audio Encoding - HBR Audio - IEC Audio Stream Packet	✓
HFI-44: Audio InfoFrame - 3D and MS Audio - Supported Frequency	✓
HFI-45: Audio Channel Status - Basic Audio - Allowed Rate	✓
<b>HDR</b>	
HFI-53: Dynamic Range and Mastering InfoFrame - High Dynamic Range	✓
<b>Read Request</b>	
HFI-17: E-DDC Protocol - Read Request - START Response	✓
HFI-20: E-DDC Protocol - Read Request - Update Flags Read	✓
HFI-23: E-DDC Protocol - Read Request - Clock Stretching	✓
HFI-27: E-DDC Protocol - Read Request - SDCS Enable Logic	✓
HFI-29: E-DDC Protocol - CED Counter Read	✓
<b>E-DDC</b>	

## HDMI 2.0 Test Results–TMDs Protocol Tests

Test Name / Details	Status
HFI-12: TMDs Protocol - 6G - Basic Protocol and Scrambling	Pass
HFI-13: TMDs Protocol - Scrambling <= 3.4Gbps	Pass

## HDMI 2.0 Test Results– Video Timing Tests

Test Name / Details	Status
HFI-14: Video Timing - 6G - 2160p 24-bit Color Depth	Incomplete
Iter 01: (96) 3840x2160p @ 50 Hz, 24 bit/Pixel	Pass
Iter 02: (97) 3840x2160p @ 60 Hz, 24 bit/Pixel	Pass
Iter 03: (106) 3840x2160p @ 50 Hz, 24 bit/Pixel	User Skipped
Iter 04: (107) 3840x2160p @ 60 Hz, 24 bit/Pixel	Fail



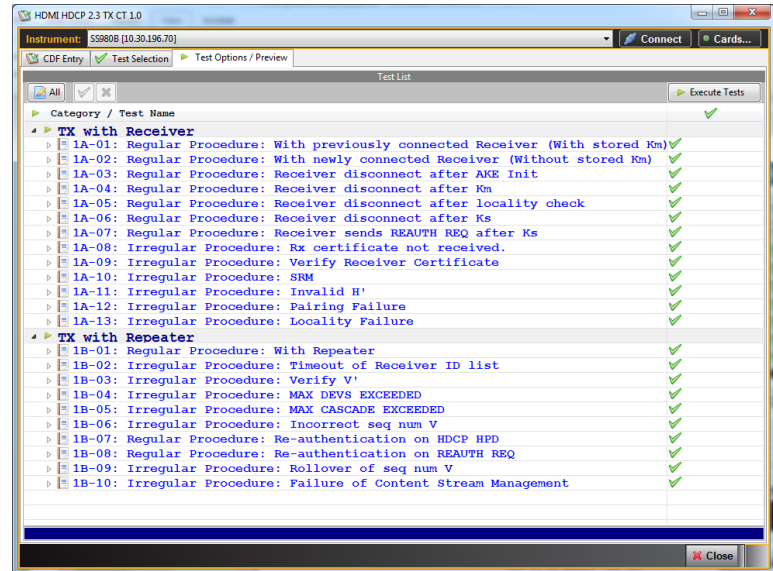
# HDCP 2.2 SOURCE, SINK, REPEATER COMPLIANCE TESTS

## HDCP 2.2 Compliance

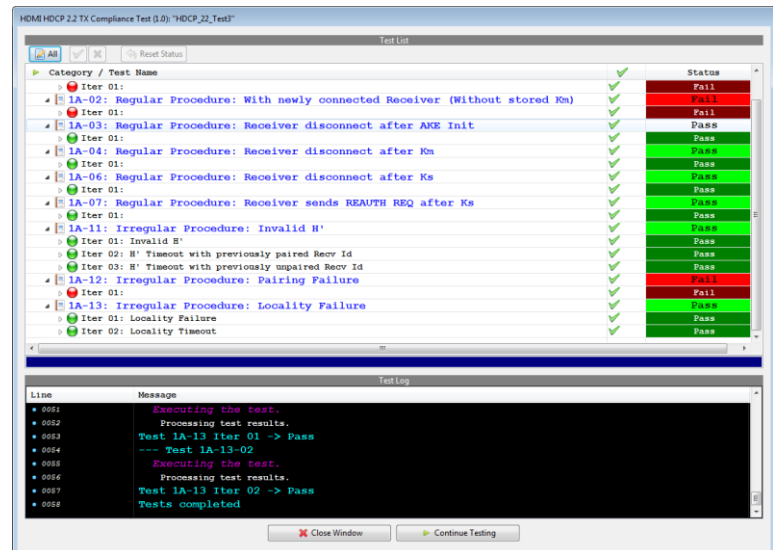
The M41h HDCP 2.2 compliance TX tests are ideal for pre-testing your HDMI source, sink or repeater product prior to submission to an Authorized Test Center for approval. Pre-testing provides assurance that your product will pass at the ATC when submitted. The compliance tests enable you to view the auxiliary channel analyzer traces logged during the test to help diagnose the cause of compliance test failures.



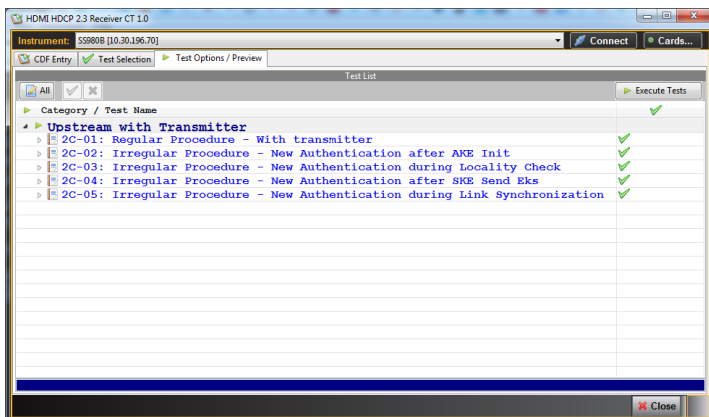
## HDCP 2.2 Test Selection – Source Tests



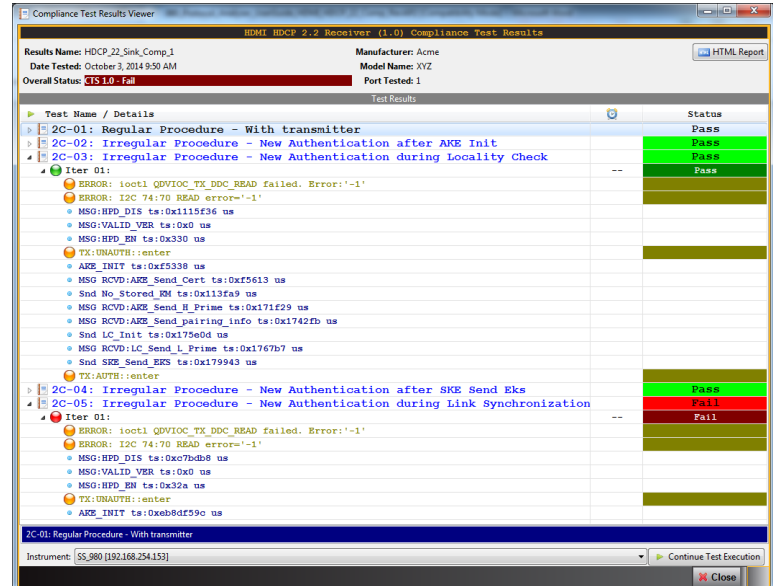
## HDCP 2.2 Test Results– Source Tests



## HDCP 2.2 Test Selection – Sink Tests



## HDCP 2.2 Test Results – Sink Tests



# SPECIFICATIONS

## HDMI Capabilities

Version	up to HDMI 2.1
Standard Formats	CEA, VESA
Protocols	FRL with FEC; TMDS, eARC Common Mode and Differential Mode
FRL bit rates	3Gbps; 6Gbps; 8Gbps; 10Gbps; 12Gbps (48Gbps aggregate)
Max Pixel Rate	1485MHz
Capture memory	8 GBytes

## Connectors - Front

HDMI Connectors (2)	In/Rx HDMI Type A; Category 2 Out/Tx HDMI Type A; Category 2
DDC Source	Used for eARC Tx EDID test
USB (2)	For connecting keyboard and mouse for ATP Manager control of external storage

## Connectors - Back

HDMI - Admin Connector	HDMI Port for M41h ATP Manager for external 4K UHD TV at Admin HDMI port
USB (2); USB-C (2)	Keyboard / mouse connected to USB ports
RJ45 E1	For admin control over LAN from computer running M41h ATP Manager
RCA (2)	SPDIF IN for injecting audio; SPDIF OUT for extracting incoming audio
BNC (2)	Trigger IN / OUT for triggering captures
All other connectors	Not used

## Physical / Electrical / Admin

Power	100-240 VAC, 50-60 Hz, 200 Watts
Weight	11.15 LBS; 5.057 Kg
Size	Height: 3.44 in. (8.74 cm) Width: 9.57 in. (24.30 cm) Depth: 10.94 in. (27.79 cm)
Rack mountable	2 RU mounts in 19 inch rack with rack mounting brackets (provided)
Internal speaker	Speaker with volume control for monitoring incoming audio
Command Line Control	Ethernet (RJ-45) for external GUI and telnet
GUI Control	Either through External PC connected over LAN to Ethernet RJ45 or: Keyboard / mouse connected to USB ports; External 4K UHD TV at Admin HDMI port
Environmental	Operating Temp: 32 to 90 (F); 0 to 32 (C)

## Ordering - Product Code

## Description

00-00258	M41h hardware and base functional unit
95-00209	M41x rack-mount kit
95-00195	Source functional test – Includes Capture Analysis and UHDA Tests
95-00201	Sink functional test - Includes UHDA Tests
95-00204	eARC Tx (Sink) functional test
95-00199	eARC Rx (Source) functional test
95-00196	FRL Source compliance tests (requires 95-00195)
95-00202	FRL Sink compliance tests (requires 95-00201)
95-00205	eARC Tx (Sink) compliance tests (required 95-00204)
95-00200	eARC Rx (Source) compliance tests (requires 95-00199)
95-00198	HDCP 2.2 Source compliance (requires 95-00195)
95-00206	HDCP 2.2 Sink compliance (requires 95-00201)
95-00197	HDMI 2.0 (2.1) & 1.4 TMDS Source compliance tests (requires 95-00195)
95-00203	HDMI 2.0 (2.1) & 1.4 TMDS Sink compliance tests (requires 95-00201)
95-00207	Sink HDR Tests (Dolby , HDR Lab) (requires 95-00201)



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