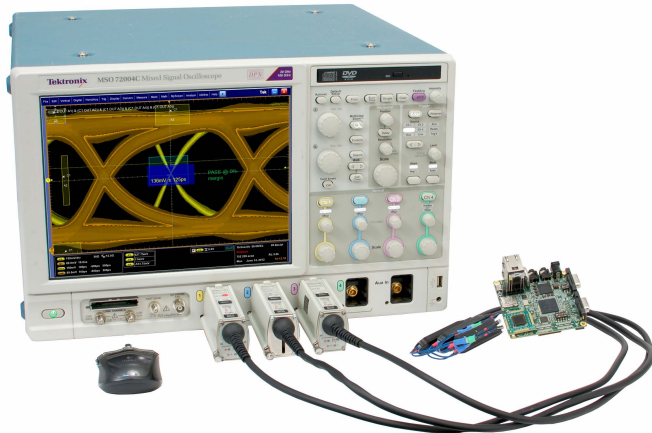# DDR5 Memory Interface Electrical Verification and Debug

## Opt. DDR5SYS - System Level Transmitter Tests Datasheet



The DDR (Dual Data Rate) is a dominant and fast-growing memory technology. It offers high data transfer rates required for virtually computing applications, from consumer products to the most powerful servers. The high speed of these signals requires high-performance measurement tools. The Tektronix TekExpress DDR Tx is an automated test application used to validate and debug the DDR5 designs of the DUT as per the JEDEC specifications. The solution enables you to achieve new levels of productivity, efficiency, and measurement reliability.

## Key features

- Supports 52 measurements of DDR5 System Transmitter Tests as per DDR5 JEDEC specification:
    - 21 Clock measurements
    - 09 Write Burst measurements
    - 01 Write Data Eye measurement
    - 13 Read Burst measurements
    - 08 Command and Address measurements
- User-Defined Acquisition (UDA) mode for Clock, Write Clock, CA, CS, Data Strobe, and data for both Write and Read traffic (or bursts).

    **UDA**: The TekExpress DDR Tx 'DDR5' Transmitter Solution puts control back where it should be, with the user. User defined acquisition mode allows you to run DDR5 JEDEC compliance measurements by customizing scope settings like sample rate, record length, bandwidth, and more
- De-embedding support for Clock, Command Address, Data Strobe, and data for both Write and Read traffic (or bursts)

- Number of UIs support for Clock and Read/Write data measurements
- Deploys DDR DFE standalone application, that can be launched from TekScope > Analyze > DDR DFE
- Support DFE for Write Data Eye measurements
- Multi-Run feature is applicable for all tests
- Save worst case waveform in known/TekExpress sessions
- Retain Vertical Scale support duringacquisition
- User-friendly measurement configurations
- Test report to reflect all the statistics of the measurement
- User can select the source and the channel in the acquisition panel
- Multiple Burst Detection Method supported - Read and Write, Write Only, Read Only, and Visual Search
- Diamond shape mask and margin analysis for Write Data Eye measurement

## Applications

Tektronix provides the most comprehensive solution to serve the needs of the engineers designing DDR silicon for server, computer, graphics systems, mobile, embedded systems, and for those who are validating the physical-layer compliance of DDR Memory Compliance Test Specification.

The Tektronix option DDR5SYS (TekExpress DDR Tx) includes compliance and debug solution for the following:

- DRAM components
- Data Buffer/RCD components
- System boards
- Embedded systems
- Servers and Client/Desktop

The Tektronix option DDR5SYS is compatible with the following Tektronix oscilloscope models:

- DPO71604SX, DPO72304SX, DPO73304SX
- Non-ATI channels of DPS75004SX, DPS75904SX, DPS77004SX
- MSO72304DX, MSO72504DX, MSO73304DX, DPO72304DX, DPO72504DX, DPO73304DX

The above-mentioned Tektronix oscilloscopes are designed to meet the challenges of the next generation memory standards and provide the industry's leading vertical noise performance with the highest number of effective bits (ENOB) and flattest frequency response for oscilloscopes in their class.

## DDR5 system level tests

The Tektronix TekExpress DDR Tx solution reduces the effort and accelerates the compliance testing for DDR systems and devices with several unique and innovative capabilities.

The TekExpress DDR Tx application provides a simple, step-by-step, and easy-to-use interface to speed up the testing process. User can select the memory technology of interest in Device, Data Rate, Burst Detection Method, select the probing configuration used for Clock, and strobe in the Setup DUT panel, in the next step perform the test selection as per measurement group (Clock, Command Address, Data Strobe, and Data for both Read and Write traffic (or bursts)) and individual measurements within the group provide different methods of Burst detection.
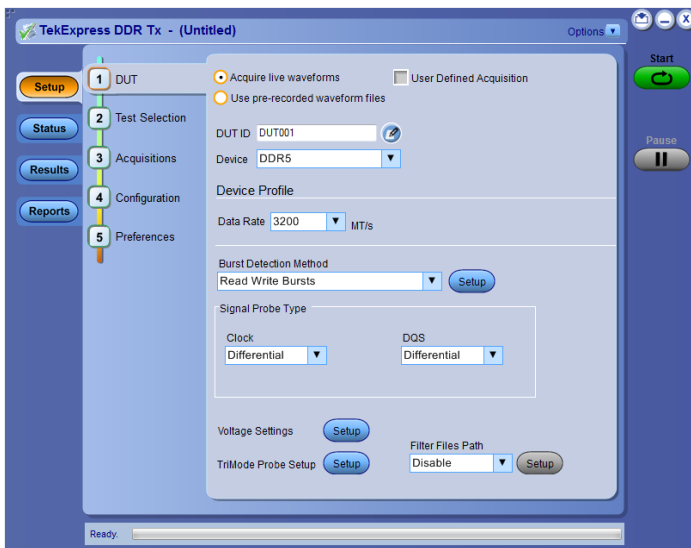


Figure 1: TekExpress DDR Tx – application launch screen

## Acquisitions

The TekExpress DDR Tx application comes with a unique feature to select or deselect the signal. Once the signal is selected in the acquisition panel, the user can select the signal source connected to the oscilloscope.



Figure 2: Acquisition panel – signal source selection

## De-embed filters

Easily de-embed the interposer and the probe effects by applying suitable de-embed filters within the DDR5 standard.



Figure 3: De-embed filters

## Comprehensive measurements

The option DDR5SYS adds a long list of JEDEC specific measurements for DDR5 memory standards. The TekExpress DDR Tx application covers Electrical measurements, Timing measurements, and Eye Diagram measurements as per the JEDEC standards.

## Automated Read and Write Burst detection

The TekExpress DDR Tx provides different ways to detect the burst cycles that are used to perform measurements:

- Read Write Bursts – when the DUT traffic is configured to send both Read and Write bursts then this method is used for burst detection.
- Write Only – when the DUT traffic is configured to send all Write Bursts then this method is used for burst detection.
- Read Only – when the DUT traffic is configured to send all Read Bursts then this method is used for burst detection.
- Visual Search – defining Visual Trigger areas to identify and gate area of interest for measurements



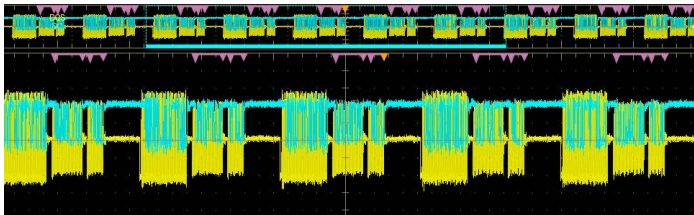*Figure 4: Burst detection*



*Figure 5: Automated Read and Write Burst detection – for Write Bursts*
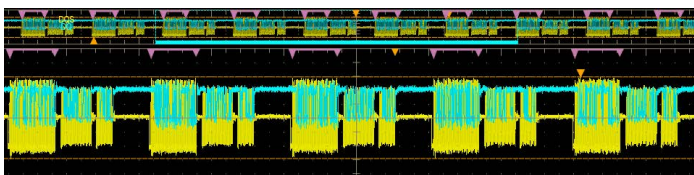


*Figure 6: Automated Read and Write Burst detection – for Read Bursts*



*Figure 7: Visual trigger*

## Test selection

The TekExpress DDR Tx test selection panel allows the user to select the various measurements supported by the application.

- Supports 52 measurements of DDR5 System Transmitter Tests as per DDR5 JEDEC specification:

  - 21 Clock measurements
  - 09 Write Burst measurements
  - 01 Write Data Eye measurement
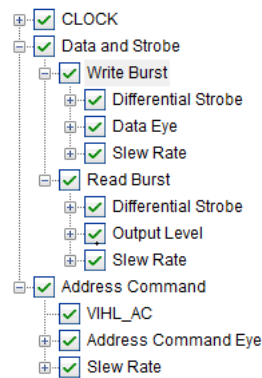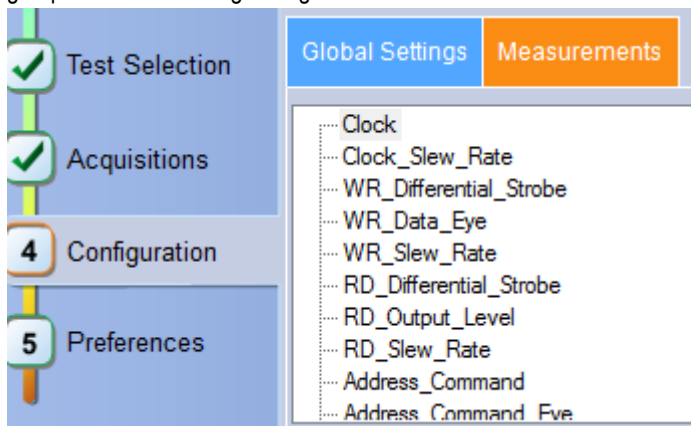  - 13 Read Burst measurements
  - 08 Command and Address measurements



*Figure 8: Test selection panel – tree view of measurements*

## Configurations

Ease of use measurement configuration to configure measurements by group instead of running through all the 50+ measurements.



## DDR DFE standalone plugin

The DDR5 application supports data rates from 3200 MT/s to 6400 MT/s. This increase in the data rate is realized without the need for differential signaling at the DQ pins i.e. the DQ bus is single-ended – same as DDR3/4. However, due to the many impedance mismatched points that exist along with the memory subsystem, ISI due to reflections are expected to increase. At data rates >= 4800 MT/s, the data eye at the DRAM ball is expected to be closed. A 4-tap DFE is implemented in the DDR5 DRAM Rx to help equalize the DQ signals and open the data eyes after the data is latched by the receiver.

The TekExpress DDR Tx application provides DDR DFE as a standalone software application in Tektronix's performance scopes. It is used to perform 4 tap DFE operation on the DDR5 write burst signals coming from the DDR5 DUTs.
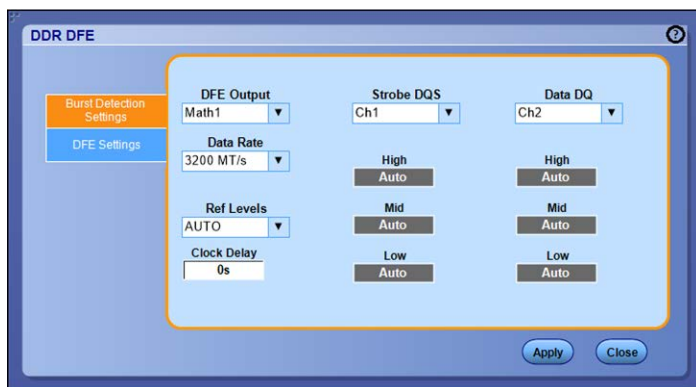


Figure 9: DDR DFE standalone plugin

## Results and reporting with waveform

The measurement configurations and JEDEC pass/fail limits are automatically applied for the selected measurements based on the memory specification and the selected speed grade. The results report includes DDR measurements statistical data, measurement plots, and the screenshot of the waveforms with the cursors. Hyperlinks within the report allows you to navigate between the sections.

When test execution is complete, the application automatically opens the Results panel and displays the summary of test results.
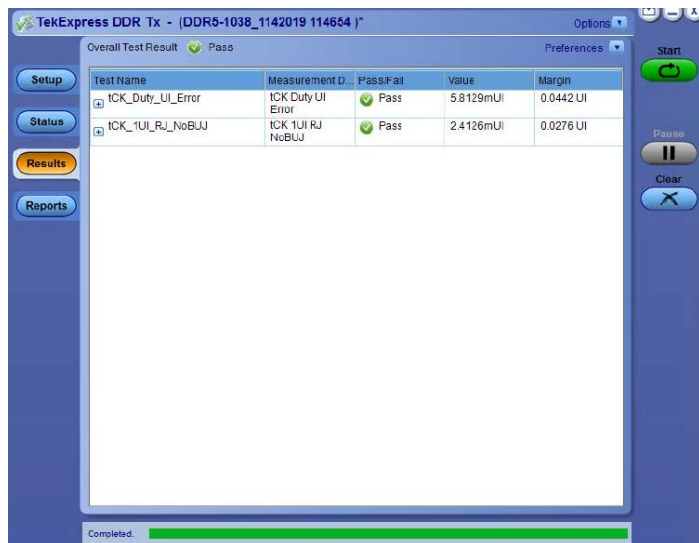


Figure 10: Measurement results



Figure 11: Measurement report

## Verification versus debug

The TekExpress DDR Tx application provides a comprehensive set of JEDEC timing and electrical measurements for the DDR5 standard. Also, it provides access to the DPOJET advanced Jitter and Timing analysis engine that allows flexibility to reconfigure the existing measurements or to perform new measurements that are not defined by the JEDEC specification using new user-specified test limits. Additionally, it features logging, filters, histograms, and time trends that are available in DPOJET. The user can also switch between debug mode and the compliance mode.

## Oscilloscope triggering and waveform identification

The Tektronix Pinpoint® trigger system provides the most comprehensive high-performance trigger system in the industry. The Pinpoint trigger system encompasses threshold and timing related triggers, Dual A and B Event Triggering, Logic Qualification, Window Triggering, and Reset Triggering.

The Advanced Search and Mark feature in the Tektronix MSO/DPO5000, DPO7000, and MSO/DPO70000 Series oscilloscopes find unique events in the waveforms. It scans acquired waveform data for multiple occurrences of an event and marks each occurrence.

The Search and Mark feature has a close relationship with the Pinpoint trigger system since they both can be used to discriminate signal characteristics. Search and Mark includes signal-shape discrimination features of the Pinpoint trigger system and extends them across live channels, stored data, and math waveforms.

The Visual Trigger makes the identification of the desired waveform events quick and easy by scanning all the acquired analog waveforms and comparing them with the geometric shapes on the display. By discarding the acquired waveforms which do not meet the graphical definition, Visual Triggering extends the oscilloscope's trigger capabilities beyond the traditional hardware trigger system.

## Supported oscilloscopes

DPO71604SX, DPO72304SX, DPO73304SX, DPS75004SX, DPS75904SX, DPS77004SX, MSO72304DX, MSO72504DX, MSO73304DX, DPO72304DX, DPO72504DX, and DPO73304DX

### Recommended probes

| Active probes | Description |
|---|---|
| P7720 | 20 GHz TriMode probe with TekFlex connector technology |
| P7716 | 16 GHz TriMode probe with TekFlex connector technology |
| **Probe tips** | **Description** |
| P77STFLXA/P77STCABL | Active, Solder-in Tip with TekFlex connector technology, probe tips to probe directly on the motherboard/vias or interposers with 0 Ω resistor. |
| P77STFLXB/P77STLRCB | Active, Solder-in Tip with TekFlex connector technology, probe tips to probe on the SI Interposer with 100 Ω resistor (Nexus XH Series Interposer). |
| SI Interposer | EdgeProbe$^{TM}$, Direct Attach, and Socketed Interposer are available from Nexus. Order directly from Nexus. Request the s-par files for all individual signals on the interposer instead of getting a generic nominal s-par model.<br><br>Refer the Nexus's page for more information:*http://www.nexustechnology.com/products/memory-interposers/ddr5-main-memory-interposers/.* |

# Ordering information

## To order a new DPO/MSO70000 Series:

| Nomenclature | Description |
|---|---|
| **SX, DX >= 16G** | |
| DPO-UP DDR5SYS | License: DDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET) |
| DPO71604SX DDR5SYS | License: DDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET) |
| DPO72304SX DDR5SYS | License: DDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET) |
| DPO73304SX DDR5SYS | License: DDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET) |
| DPS75004SX DDR5SYS | License: DDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET) |
| DPS75904SX DDR5SYS | License: DDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET) |
| DPS77004SX DDR5SYS | License: DDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET) |
| DPO72304DX DDR5SYS | License: DDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET) |
| DPO72504DX DDR5SYS | License: DDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET) |
| DPO73304DX DDR5SYS | License: DDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET) |
| MSO72304DX DDR5SYS | License: DDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET) |
| MSO72504DX DDR5SYS | License: DDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET) |
| MSO73304DX DDR5SYS | License: DDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET) |

## To order floating licenses on existing DPO/MSO70000 Series:

| Product Nomenclature | Description | Mapped Options | Required Options |
|---|---|---|---|
| DPOFL-DDR5SYS | License; DDR5 System-level Tx TekExpress Compliance/ Debug Automation Software; Floating | DDR5SYS | SDLA64, DJA, and VET |
| DPOFT-DDR5SYS | License; DDR5 System-level Tx TekExpress Compliance/ Debug Automation Software; Floating Trial | DDR5SYS | SDLA64, DJA, and VET |

Tektronix is registered to ISO 9001 and ISO 14001 by SRI Quality System Registrar.

Product(s) complies with IEEE Standard 488.1-1987, RS-232-C, and with Tektronix Standard Codes and Formats.

**GPIB**
IEEE-488

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